Next Generation Compton Telescope Design Challenges

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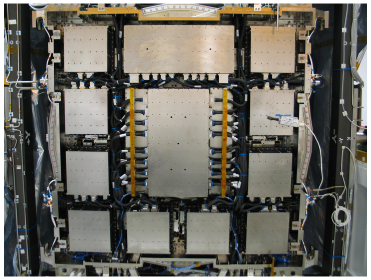
LAT Lessons for MeV Missions

❑ Minimize passive material in and around detectors but survive launch loads	Eng Model Tracker Tower did not survive vibration tests, structural mount had to be redesigned
❑ Getting rid of heat – Removing heat from detectors – Managing large radiators	Temp gradient in tracker towers required active cooling during ground testing to protect assemblies. Spent ~$10M on flight VCHP radiators and control system
❑ Application Specific Integrated Circuits / Electronics – Design and test cycle is slow – Qualifying design and parts for space and radiation enviroment – Encapsulation (plastic carriers) or chip-on-board become qualification and assembly headaches – Hi-reliability electronic parts are not readily available, particularly in 3.3V and 2,5V logic, ADCs, DACs, etc	LAT needed total of 16,000 ASICS in 10 applications. Multiple revisions on front end ASICs created significant schedule delay LAT needed to qualify ~10,000 plastic-encapsulated ADCs and DACs
❑ Space-qualified Computing is not state-of-the-art 	5 BAE Rad750 computers (including redundancy) were required to handle data volume (10k events/sec), perform background rejection and data compress to the available 400Hz event rate to the ground.

R&D Needs

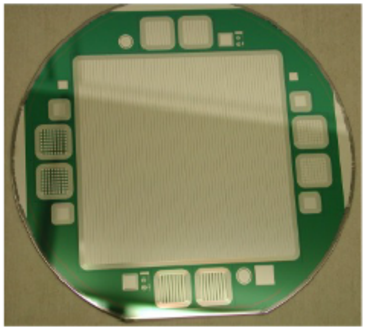
Current State of the Art Designs

- ❑ Detector:
  - 6-inch wafers
  - 2 mm thick
  - 2 mm guard rings
- ❑ ASIC:
  - Custom ASIC design with Brookhaven National Laboratory

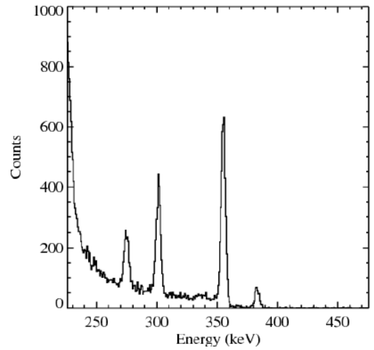
Long Term Developments

- ❑ Detectors:
  - Larger (200 mm wafers)
  - Thicker (Trenched)
  - Edgeless

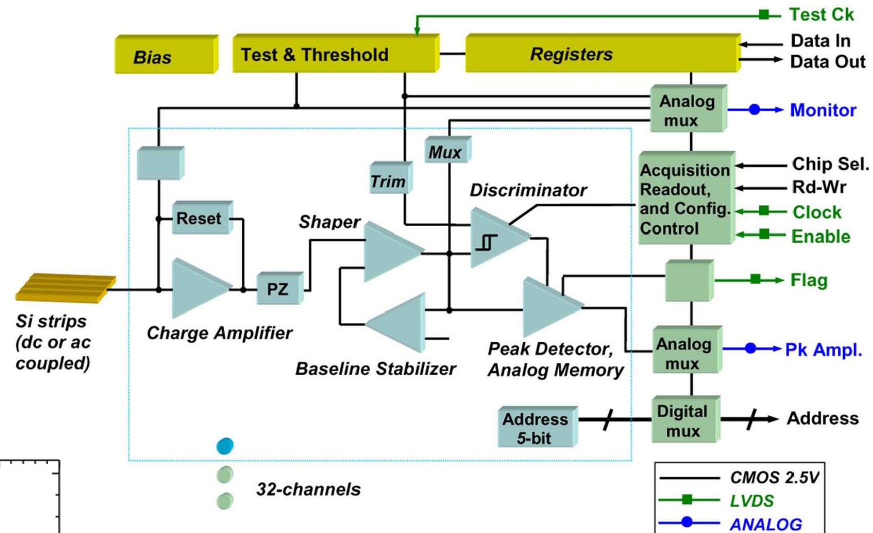
Silicon Compton Telescope Progress



Silicon strip detector on a 150 mm dia. wafer.

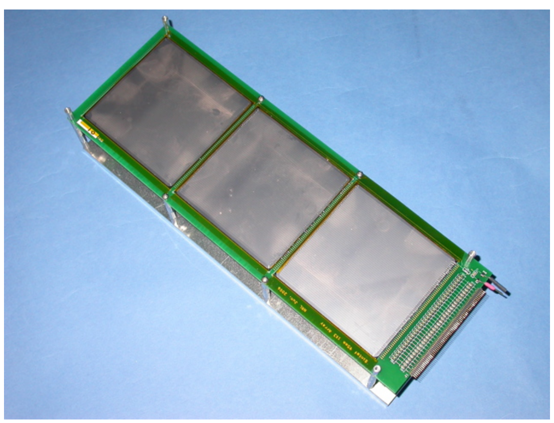


Spectrum of a ^{133}Ba source with ~4 keV FWHM resolution



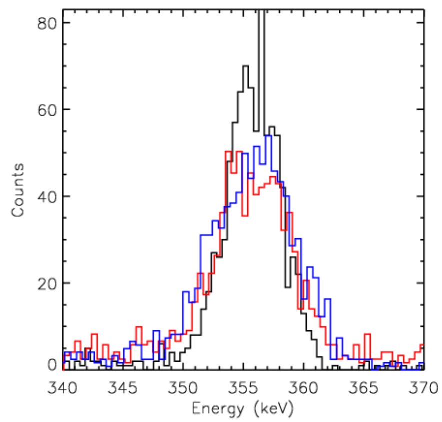
Si Strip Detector ASIC [De Geronimo, et al. 2008]

- 32 channels – pos/neg polarity
- 200 e- RMS at 30 pF
- 400:1 dynamic range
- Peak Detect and memory
- Readout mux
- 5 mW per channel



3 9-cm detectors in series

64 strips (1.4 mm pitch).



^{133}Ba line (356 keV) for 1 (**black**: 5.2 keV), 2 (**red:** 6.8 keV) and 3 (**blue:** 7.6 keV) detectors coupled together.

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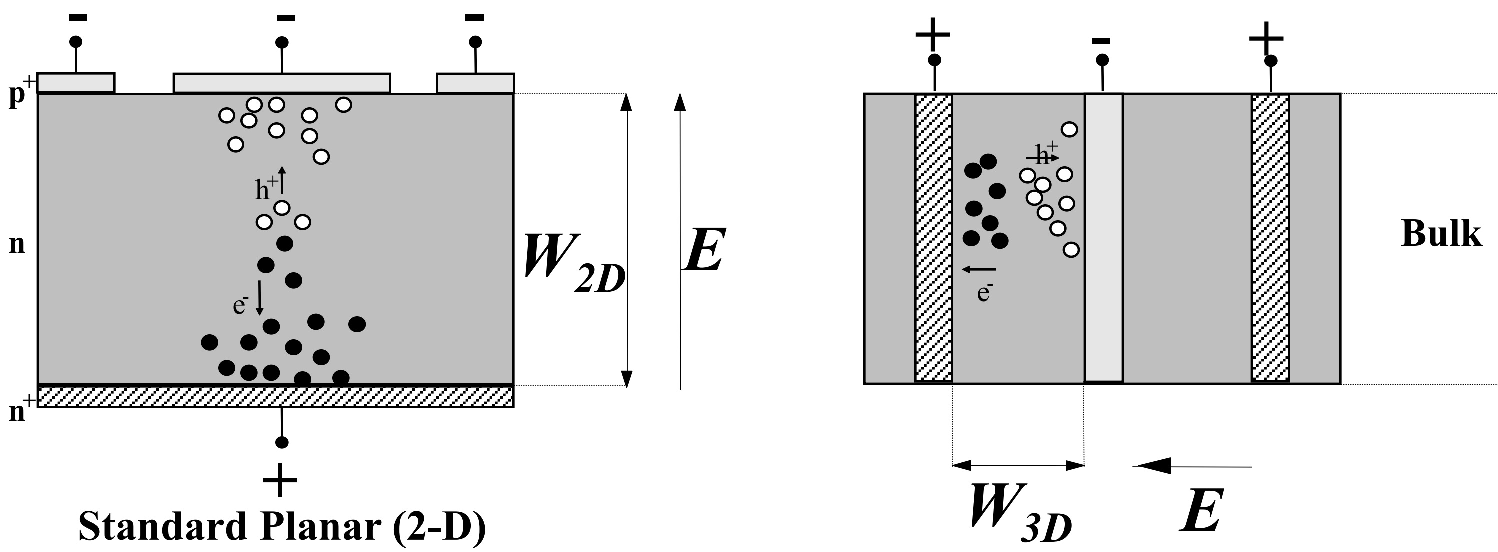
Long Term Developments

- ❑ Detectors:
  - Thicker (Trenched) silicon detector
  - Larger (200 mm wafers) silicon detector
  - Edgeless silicon detector
  - Better scintillator

Standard 3-Dimensional Detectors



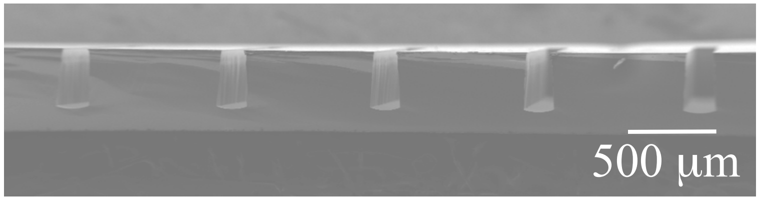
S.I. Parker, C. J. Kenney, J. Segal,
Nucl. Instr. Meth. Phys. Res. A 395 (1997) 328

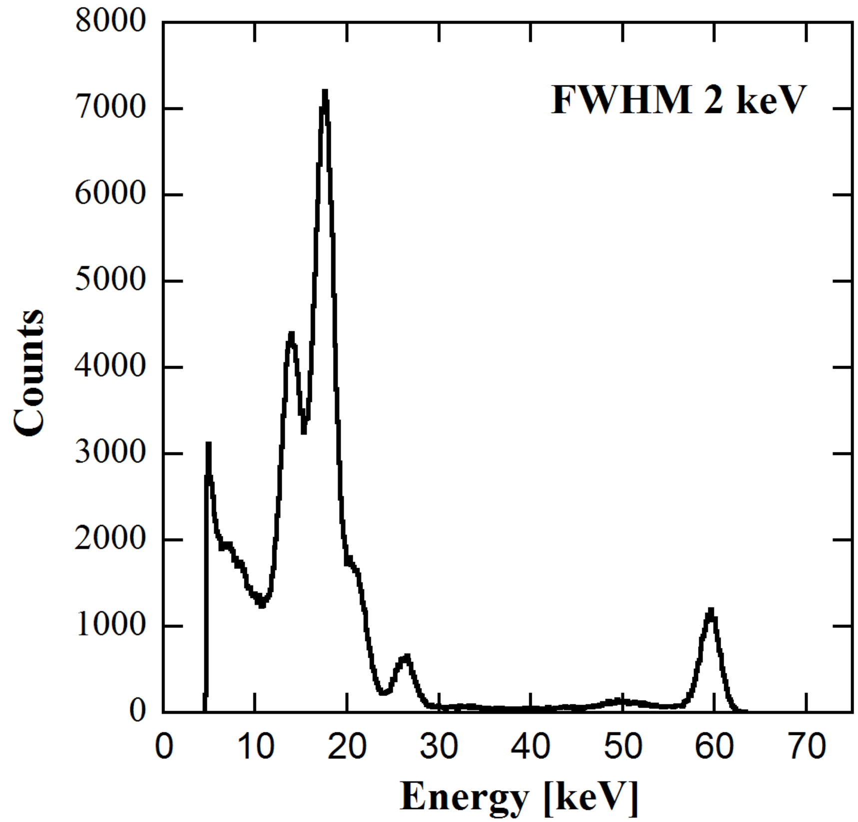
Short distance between electrodes:

- low full depletion voltage
- short collection distance
- more radiation tolerant than planar detectors!

DRAWBACK: Fabrication process of 3-D devices is not standard.

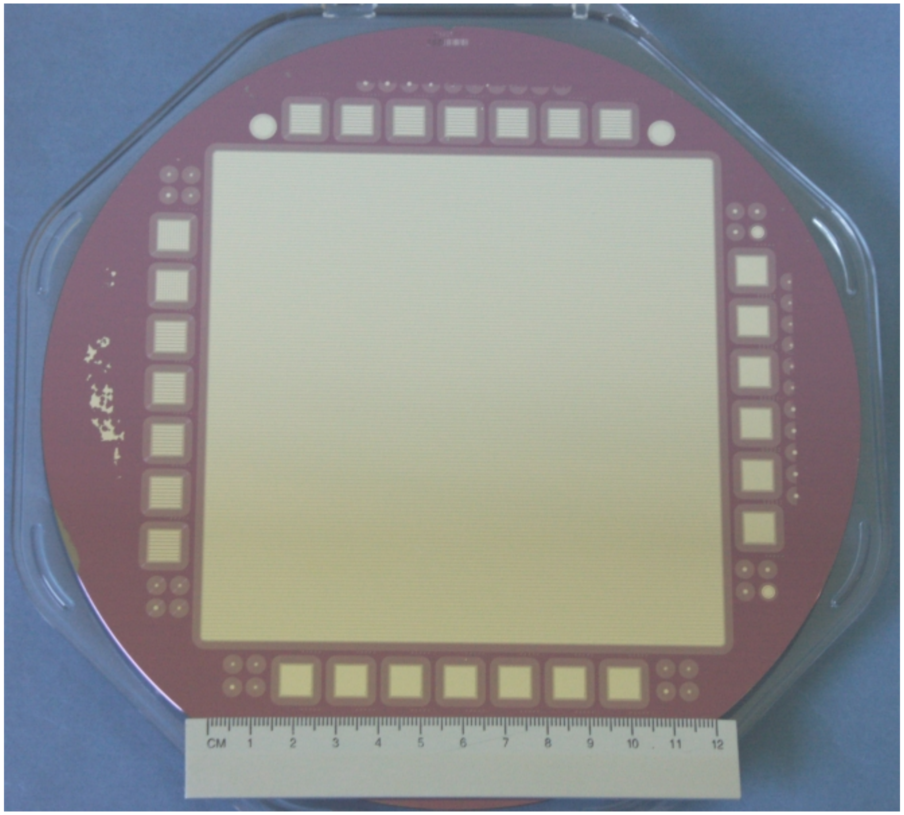
Am-241 Spectrum





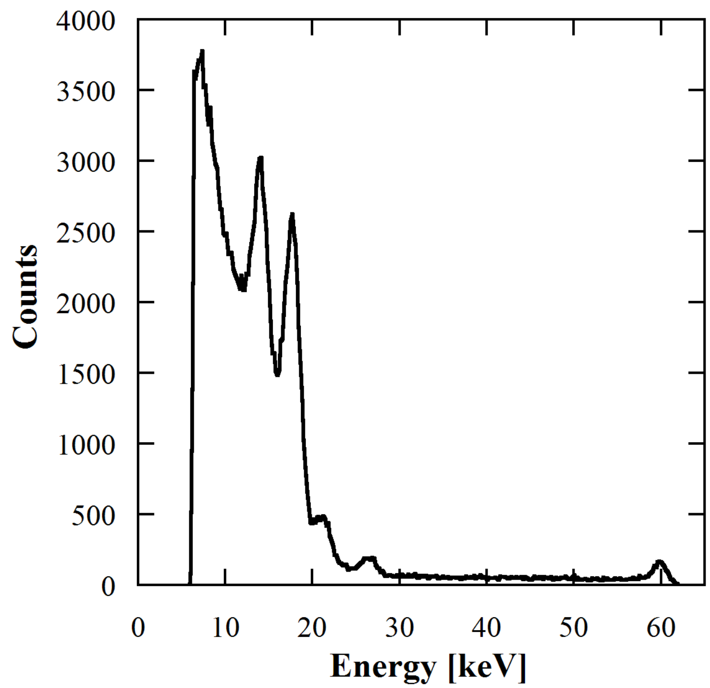
- ^{241}Am source
- energy resolution is ~ 2.3 keV FWHM at 59.5 keV
- excellent charge collection

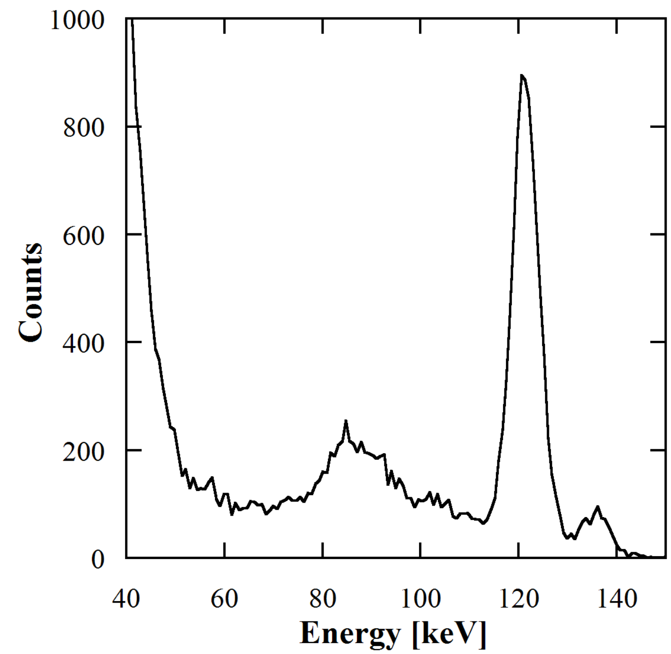
Larger Detectors



- Develop detectors from 200 mm (8-inch) wafers
  - 9,000 Ohm-cm material
  - 725 microns thick, 128 strips, each 125 mm x 0.97 mm
- Effective area: 156 cm^2

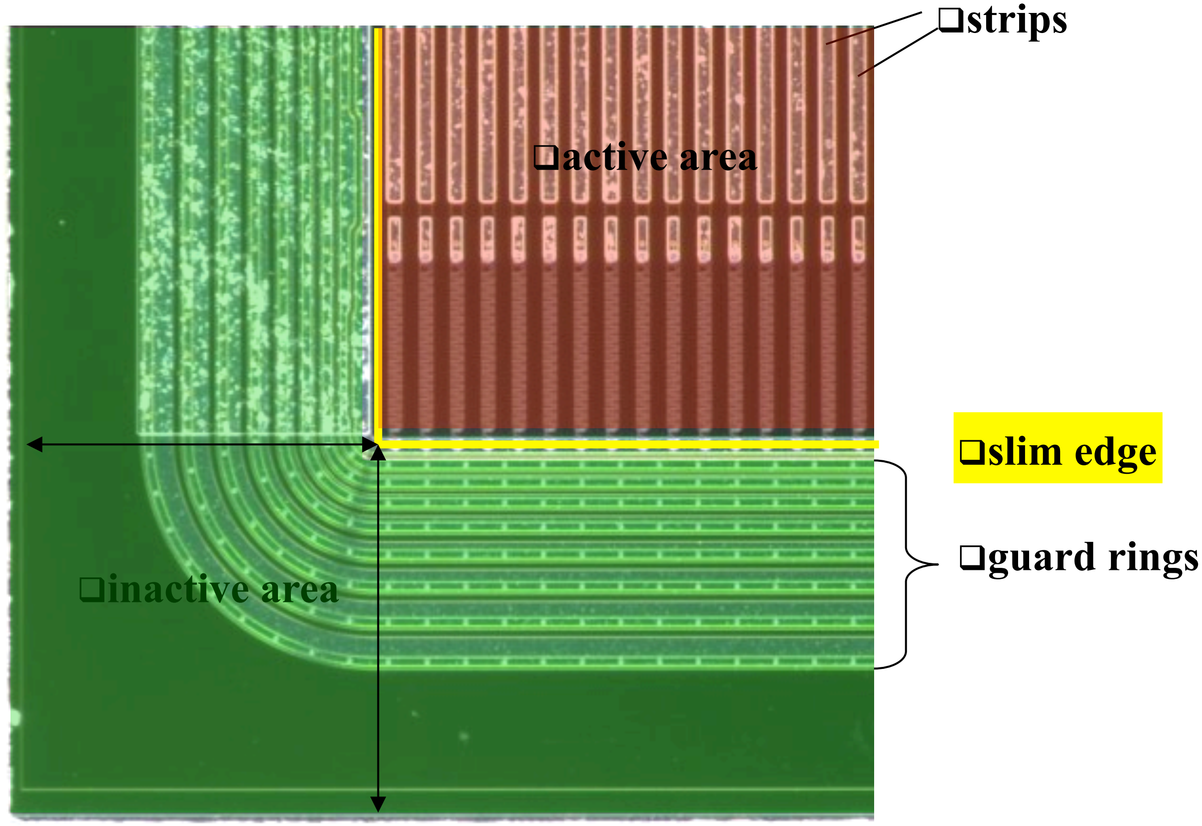
200 mm Wafer Results





- Performance demonstrated
- Large number of bad strips
- Would need dedicated fab for good yield

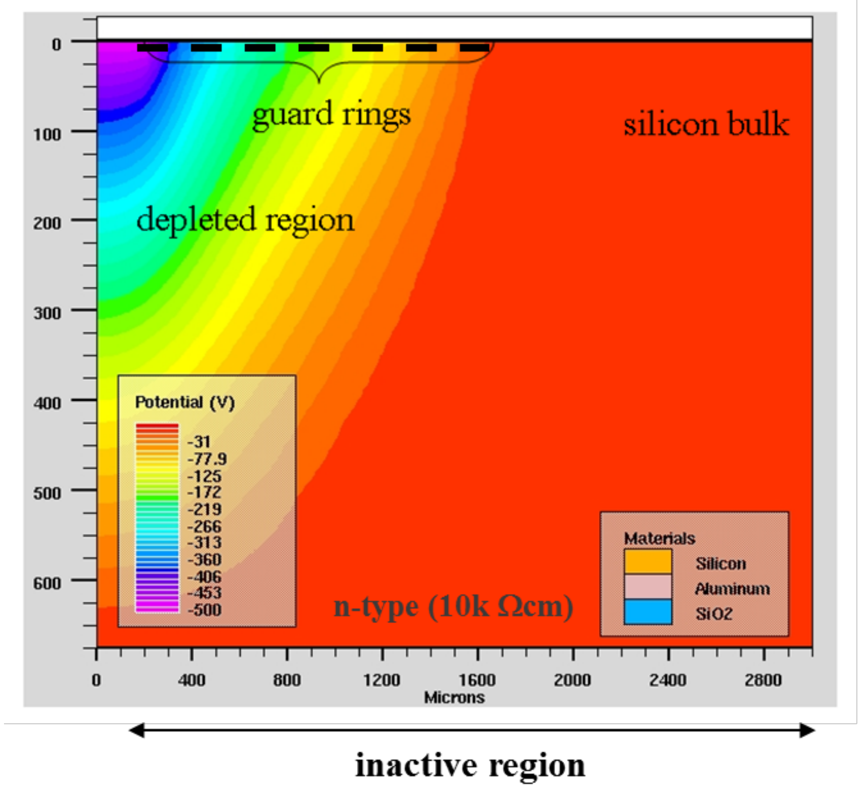
Edgeless Detectors

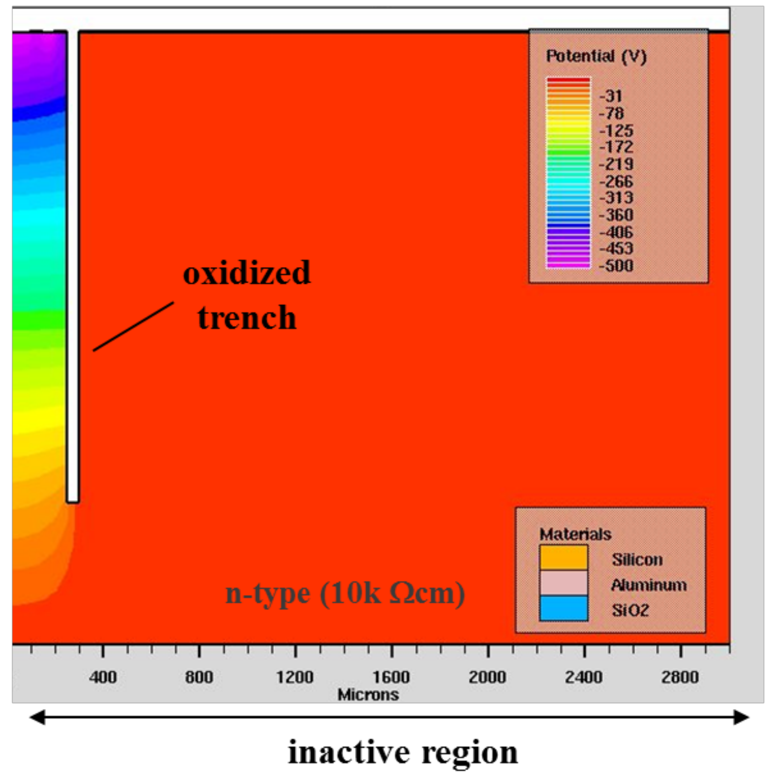


❑Optical micrograph

- Edges are significant amount of passive mass
- Can make detectors without edges
- Research being used by RD-50 for ATLAS upgrade at CERN

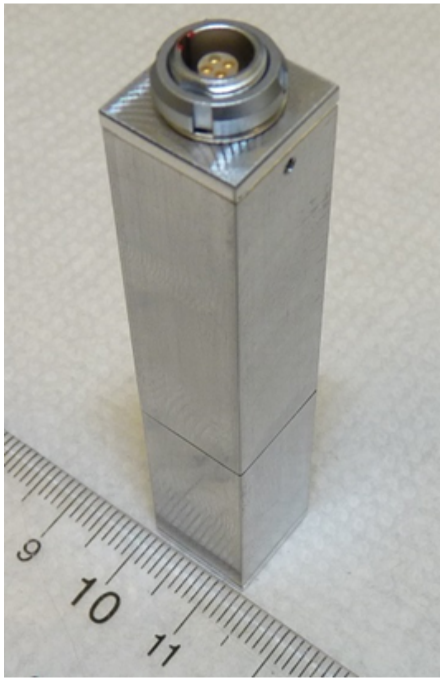
Edgeless Detectors

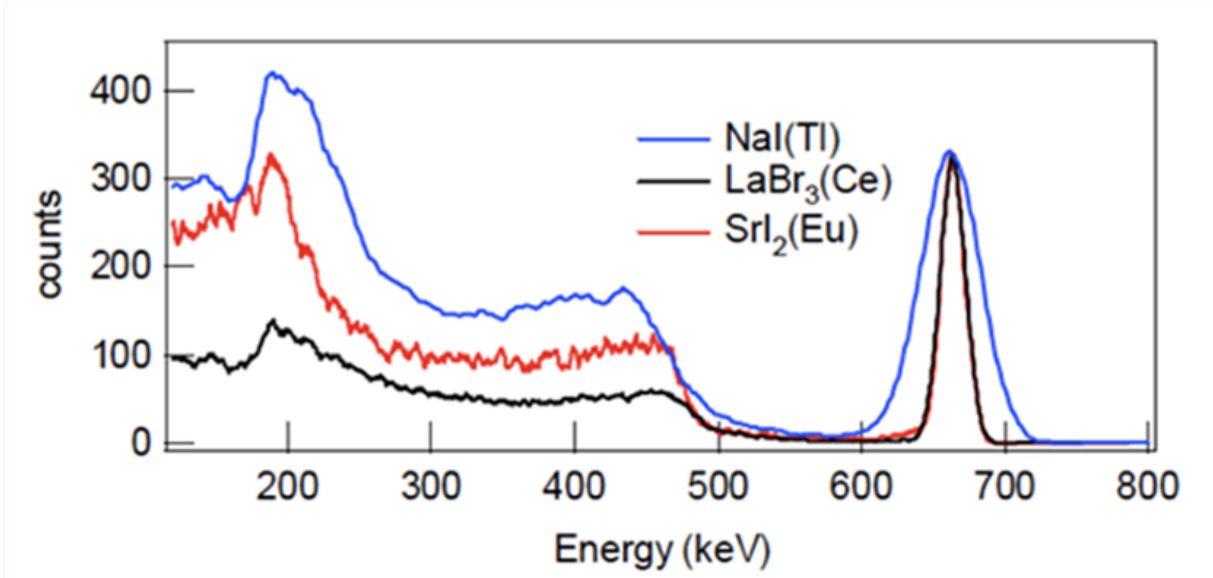




- By adjusting surface charge on the edge of the detector, the right field can be achieved without guard rings.
- Made possible by Atomic Layer Deposition
- Have achieved dead regions of few microns on 300 micron-thick device

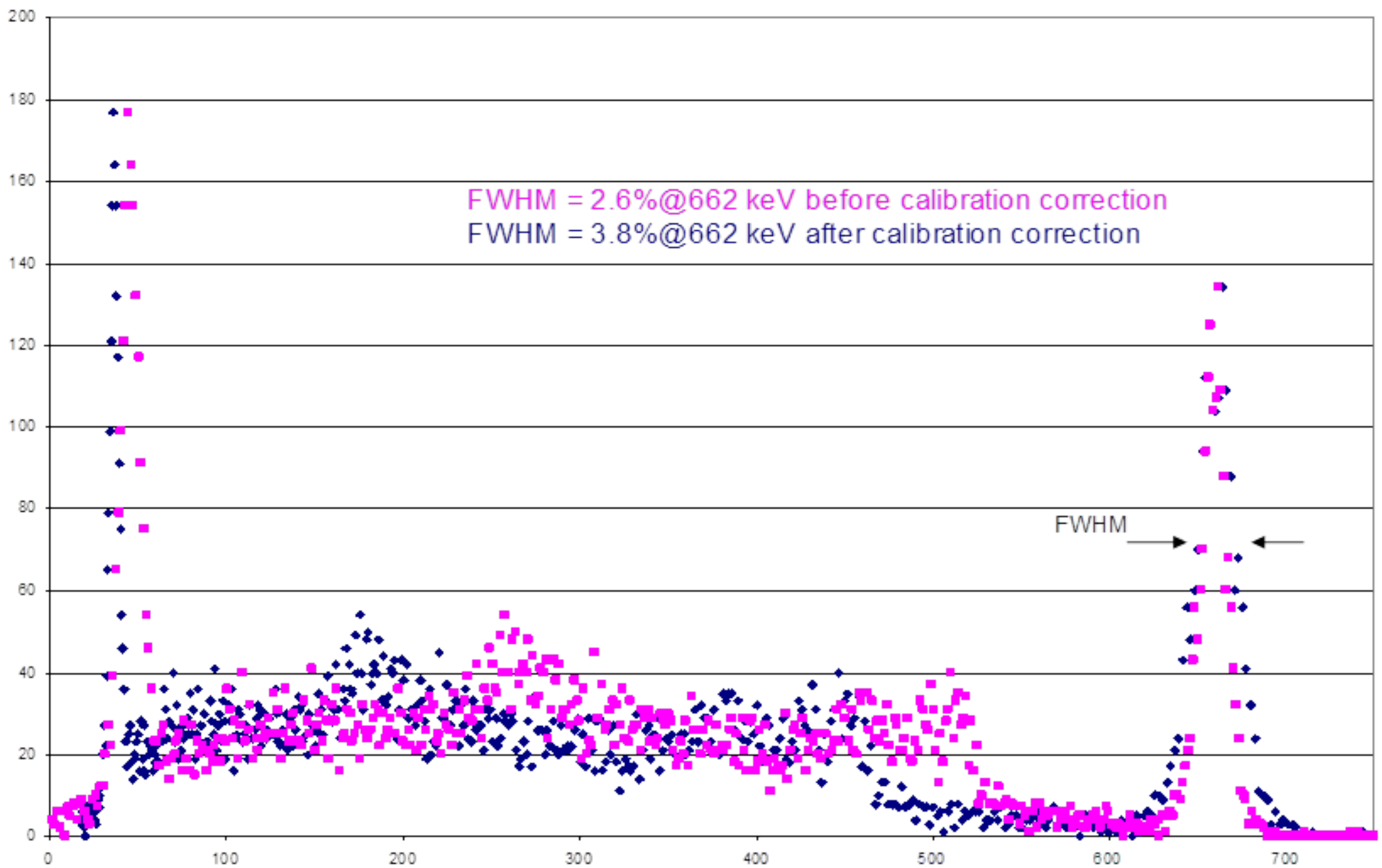
SrI-SiPMT Scintillation Detectors





- SrI new scintillator with good energy resolution and low background (unlike LaBr)
- Made SrI "pixel" detectors and read out with Si-PMT
- Will be space qualified in 2016
- Manifested for launch on DoD STP-Sat5 (NRL SIRI experiment)
  - Polar orbit
  - 1 year mission

SrI-SiPMT Spectra



- Detector non-linearity must be corrected
- Achieve 3.8% energy resolution at 662 keV

Conclusions

- Current state of the art:
  - Silicon: 6-inch, 2 mm thick
  - Scintillators: NaI, CsI, …

Go with this, or improve basic detector technology?

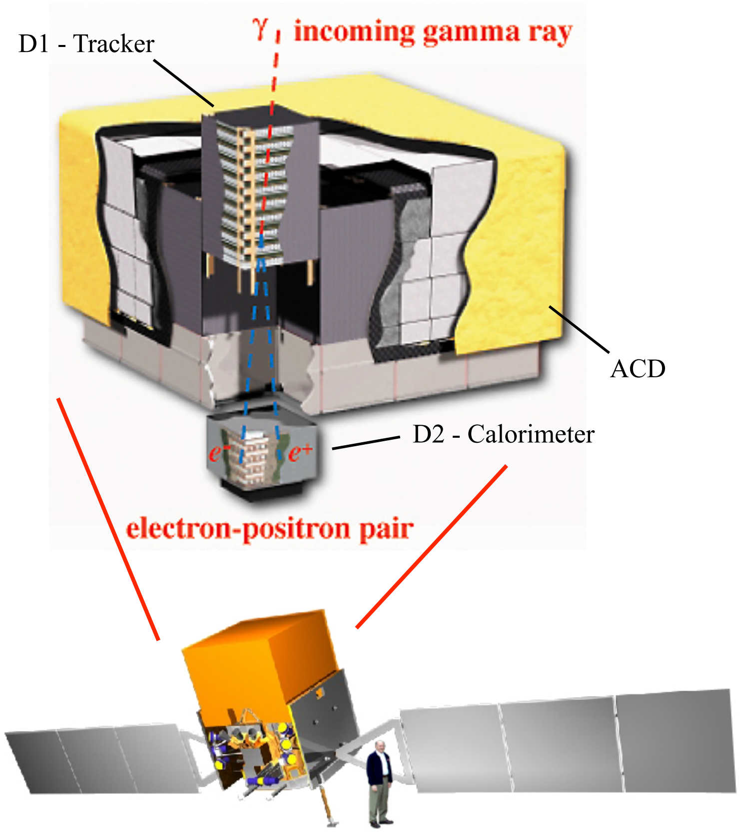
- Larger, thicker, edgeless silicon detectors
- Other semiconductors? (CdTe, CdZnTe, InP)
- Other Scintillators? (SrI, NaI,…)

Backup Slides

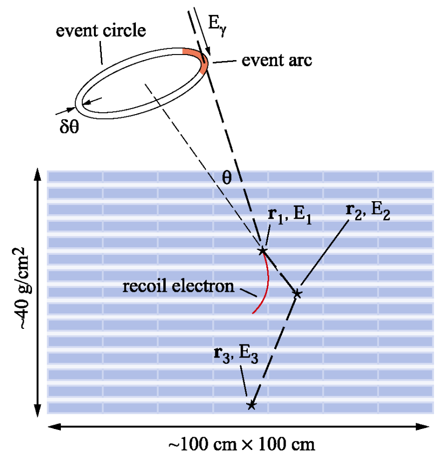
Advanced Compton Telescope (ACT)

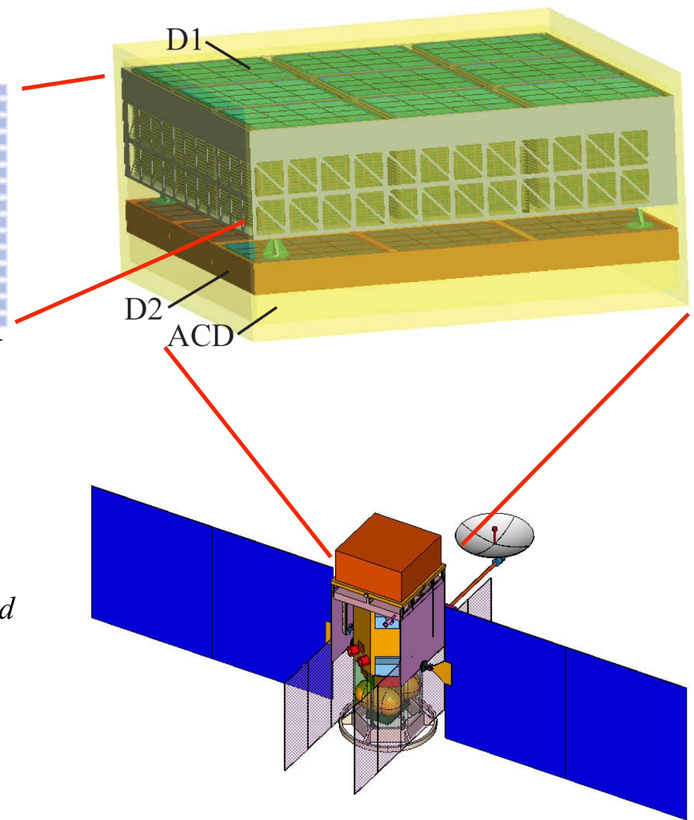
Boggs, et al. 2006 (arXiv:astro-ph/0608532v1)

GeV γ's – Pair Telescope



MeV γ's – Compton Scatter Telescope

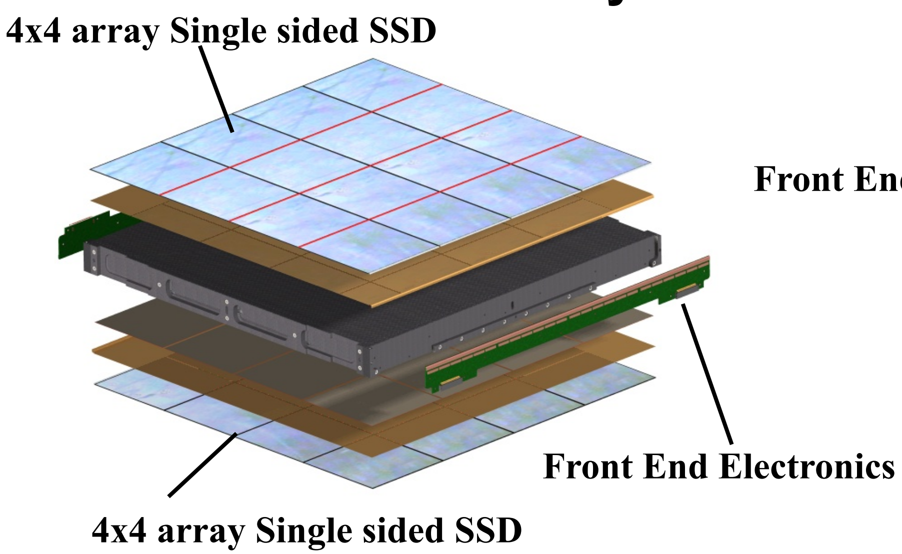




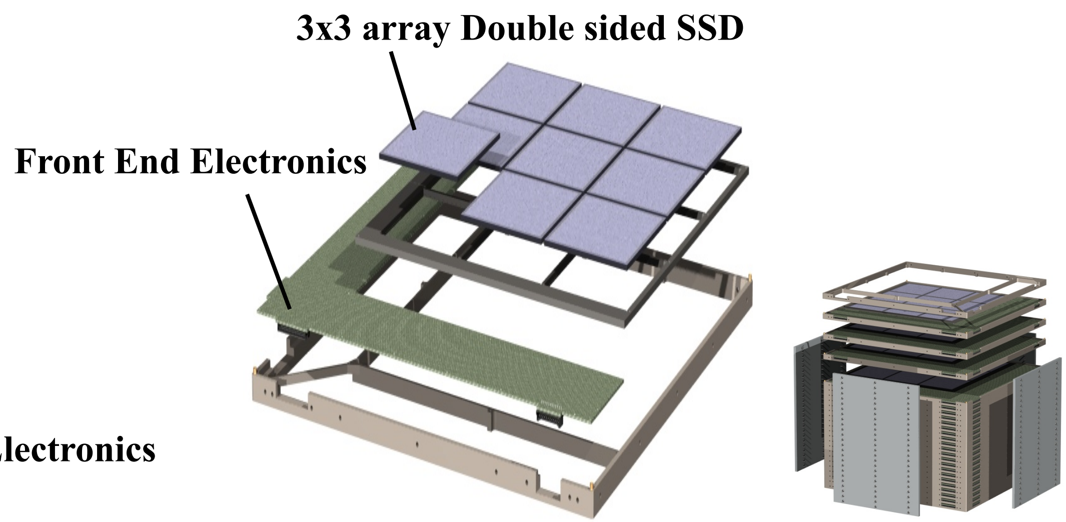
Array of highly segmented semi-conductor detectors (eg. Ge, Si, or CdTe) record the position and energy deposition of interactions to reconstruct incident photon direction and energy

Challenges of Silicon Compton

LAT Tracker Tray



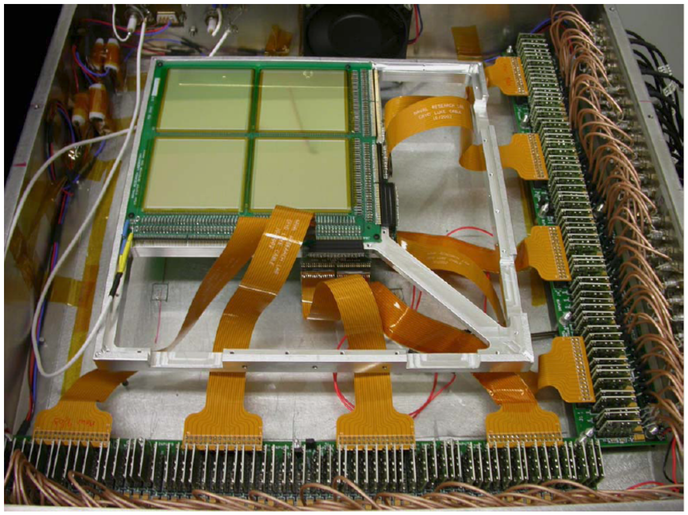
Silicon Compton Tray

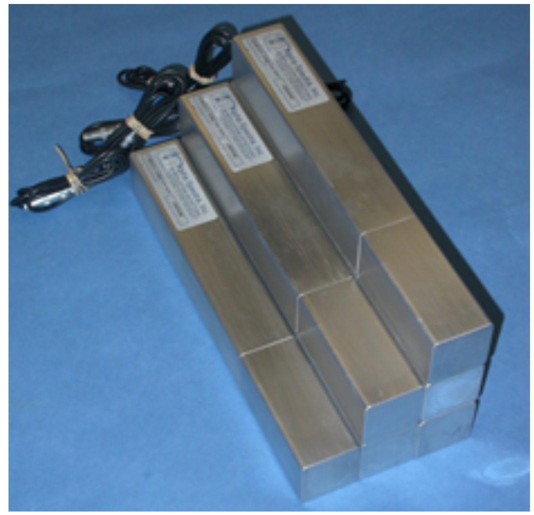


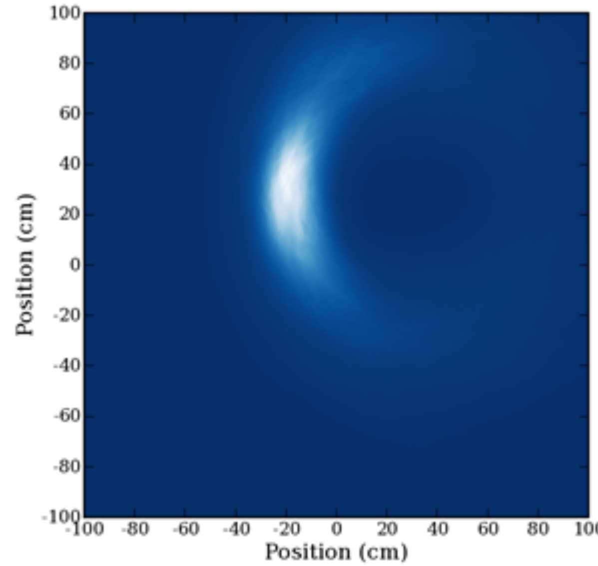
- Silicon Compton requires double-sided strip detectors to position the Compton interactions in a single crystal
- Preferred detector thickness is 2 mm or greater
  - Higher depletion voltages
  - Higher quality silicon material

- Requires spectroscopy of events in silicon
  - more complex front ends
  - Pulse amplitude measurement
- Performance improves with lower energy threshold – better noise performance
- Fewer channels but likely higher power per channel

Si-NaI Prototype





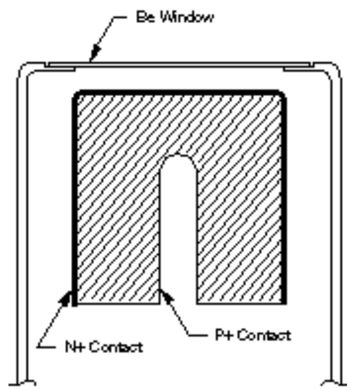


Thick Trenched Gamma-Ray Detectors

Thick Silicon Strip Detectors via Microfabrication

**Marc Christophersen,
Bernard Phlips, and Francis J. Kub
NRL**

- Method to develop thicker silicon detectors by changing planar charge collection geometry
- Thick devices deplete at much lower bias voltages
  - Enables consideration of lower quality material
- The same principle could be applied to other semi-conductors, e.g. CdTe, CdZnTe, or InP.
  - The short carrier lifetime can be overcome by “charge–mining” with the trenches.



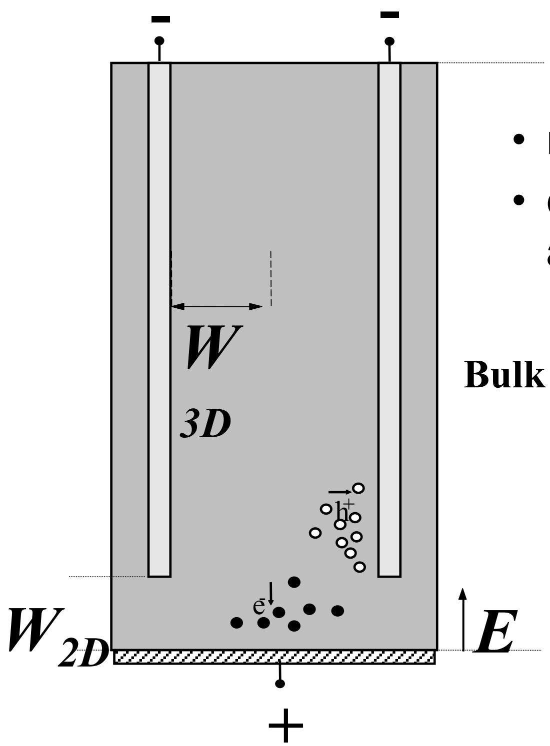
Coaxial Ge Detector

NRL’s NanoScience Institute

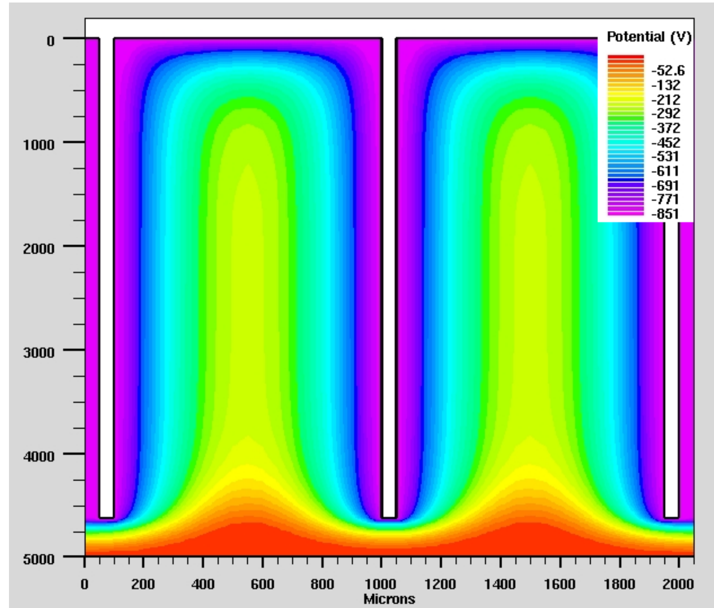
Class 100 Cleanroom
5000 ft^2

- SEM (scanning electron microscope)
- pattern generator
- mask aligner
- reactive ion etcher (RIE) & DRIE
- e-beam evaporator

Trenched Gamma-Ray Detector - Concept



- mm thick detectors
- decouple thickness and depletion voltage



Silvaco® simulation result

Our goal:

5 mm thick trenched detector with near trenches for lateral depletion and charge collection.

Fabrication Challenges:

- Microfabrication – high-aspect ratio trench/ hole arrays, millimeters deep
- Junction formation – homogeneous junction (no ion-implantation, I2)
- Leakage currents – maintain high minority carrier lifetime

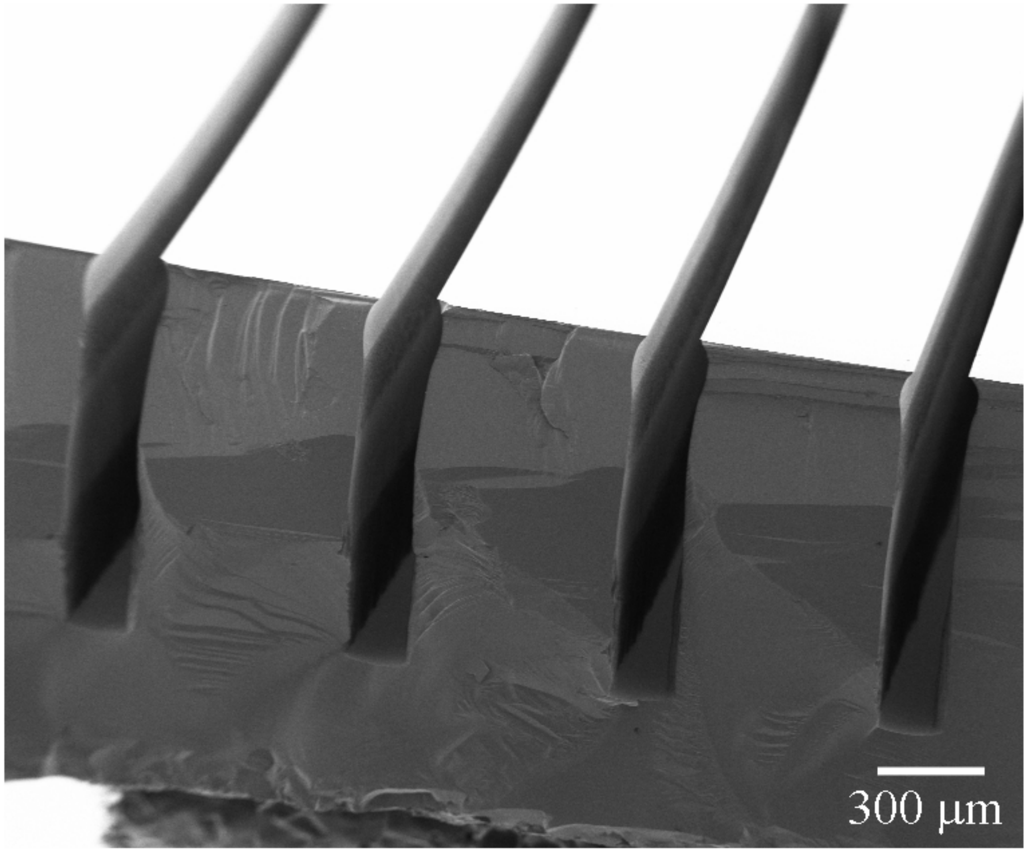
Si Compton Design Drivers

- ❑ Commensurate energy resolution and position resolution for best Compton reconstruction.
  - mm positions, few keV energy resolution
- ❑ Minimize passive material in the detection volume
  - Passive material produces tails on the Point Spread Function, or
  - Results in loss of effective area, incorrect Compton reconstruction
- ❑ Minimize power
  - Power is expensive and large areas become problematic in launch and deployment
  - Related heat within the instrument is difficult to remove

➢ **Maximize silicon depth and length of strip readout with single electronics chain, commensurate with requirements for max capacitance, single scatter in volume and Compton electron tracking desires.**

5 mm thickness of Si strip detectors is near optimal

Silicon DRIE (Deep Reactive Ion Etching)

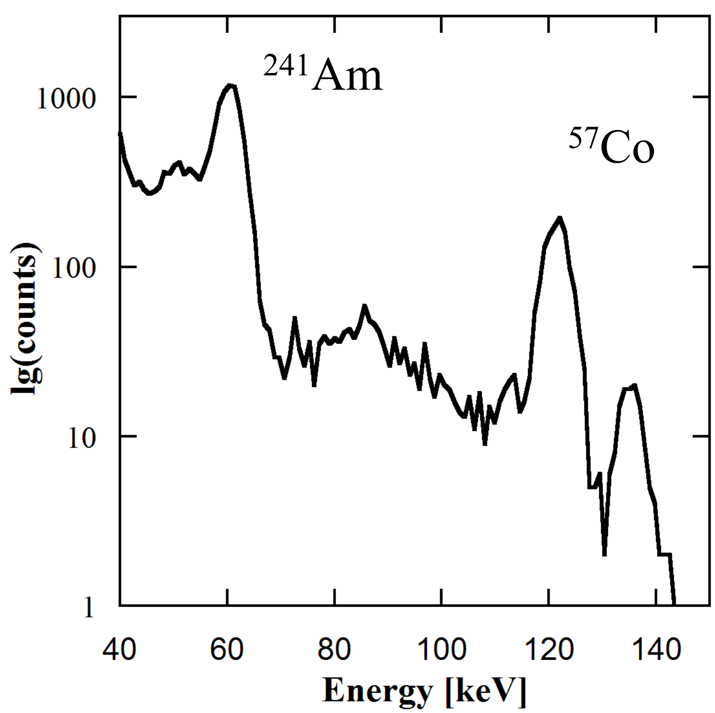


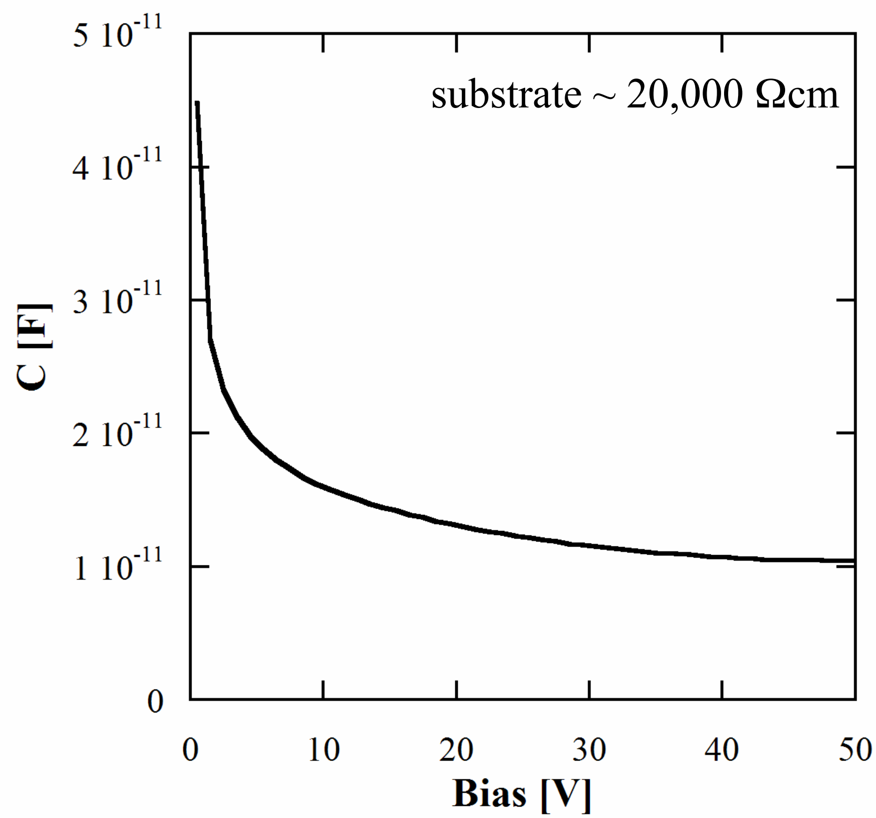
SEM micrograph, bird's-eye-view.

aspect ratio ~ 12

Final devices will have narrower trench arrays.

2-mm Thick Wafer





Energy resolution: 3.0 keV FWHM at 60 keV

Full depletion at 50 V.

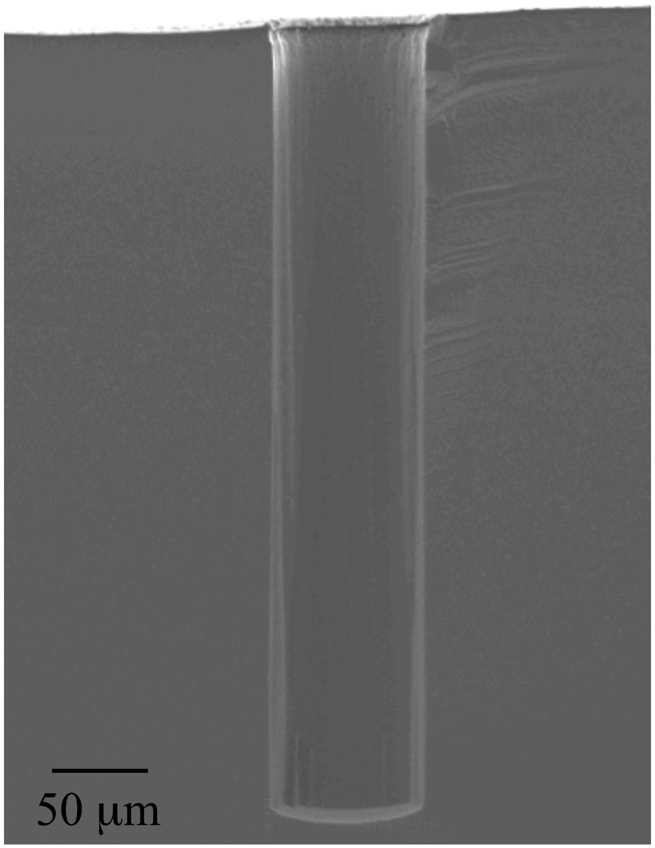
Silicon DRIE (Deep Reactive Ion Etching)

"Types" of deep anisotropic etching:

- Bosch process,
- Room T continuous process,
- cryogenic process.

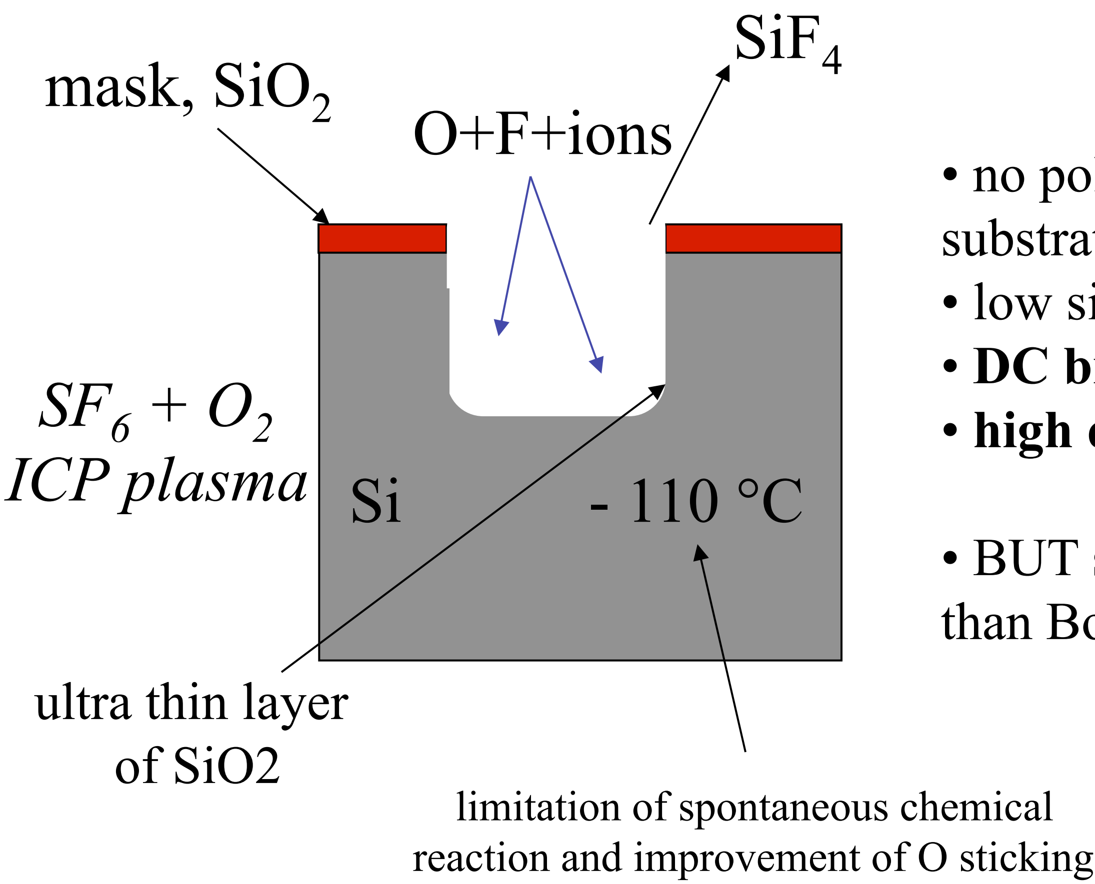
maximal reported depth 300 – 600 μm
(wafer through and via etching)

A. Ayon et al., *Sens. Act. A*, 91, 2001



SEM cross-section micrograph

Cryogenic DRIE



- no polymer contamination (reactor, substrate) in comparison to Bosch,
- low sidewall roughness,
- **DC bias < 10 V** (no silicon damage)
- **high etch selectivity** ~ 500 – 1,000 to SiO_2,

- BUT sensible process and not so flexible than Bosch process!